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Terms	Documents
(deadlock or livelock) same bus same (bridge or expansion)	116

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

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Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L1	(deadlock or livelock) same bus same (bridge or expansion)	116	L1

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Terms	Documents
L1	0

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

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DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=USPT; PLUR=YES; OP=OR			
L1	(deadlock or livelock) same bus same (bridge or expansion)	116	L1

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Terms	Documents
(710/110)!.CCLS. or 710/107.ccls. or 710/263.ccls. or 710/41.ccls. or 710/52.ccls. or 709/100.ccls. or 709/208.ccls. or 714/47.ccls. or 711/151.ccls.	3698

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

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Search History

DATE: Tuesday, January 21, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L3	(710/110)!.CCLS. or 710/107.ccls. or 710/263.ccls. or 710/41.ccls. or 710/52.ccls. or 709/100.ccls. or 709/208.ccls. or 714/47.ccls. or 711/151.ccls.	3698	L3
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=USPT; PLUR=YES; OP=OR			
L1	(deadlock or livelock) same bus same (bridge or expansion)	116	L1

END OF SEARCH HISTORY

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Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L1 and L3	36

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear

Search History

DATE: Tuesday, January 21, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L4	L1 and L3	36	L4
L3	(710/110)!.CCLS. or 710/107.ccls. or 710/263.ccls. or 710/41.ccls. or 710/52.ccls. or 709/100.ccls. or 709/208.ccls. or 714/47.ccls. or 711/151.ccls.	3698	L3
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=USPT; PLUR=YES; OP=OR			
L1	(deadlock or livelock) same bus same (bridge or expansion)	116	L1

END OF SEARCH HISTORY

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(deadlock or livelock) and (bridge or expansion) and (transaction or task or job)

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Deadlock-free scheduling of flexible manufacturing systems based or heuristic search and Petri net structures**
Mu Der Jeng; Wan Der Chiou; Yuan Lin Wen;
Systems, Man, and Cybernetics, 1998. 1998 IEEE International Conference on
Volume: 1 , 11-14 Oct 1998
Page(s): 26 -31 vol.1

[Abstract] [PDF Full-Text (452 KB)] **IEEE CNF**

2 **An acyclic expansion algorithm for fast protocol validation**
Kakuda, Y.; Wakahara, Y.; Norigoe, M.;
Software Engineering, IEEE Transactions on , Volume: 14 Issue: 8 , Aug 1988
Page(s): 1059 -1070

[Abstract] [PDF Full-Text (1000 KB)] **IEEE JRN**

3 **Performance analysis of two-phase locking**
Thomasian, A.; Ryu, I.K.;
Software Engineering, IEEE Transactions on , Volume: 17 Issue: 5 , May 1991
Page(s): 386 -402

[Abstract] [PDF Full-Text (1576 KB)] **IEEE JRN**

4 **Recursive cube of rings: a new topology for interconnection network**
Sun, Y.; Cheung, P.Y.S.; Lin, X.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 11 Issue: 3 , 2000
Page(s): 275 -286

[Abstract] [PDF Full-Text (1112 KB)] **IEEE JRN**

5 **High-performance routing in networks of workstations with irregular topology**
Silla, F.; Duato, J.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 11 Issue: 7 , 2000
Page(s): 699 -719

[Abstract] [PDF Full-Text (540 KB)] **IEEE JRN**

6 **A protocol for deadlock-free dynamic reconfiguration in high-speed l area networks**
Casado, R.; Bermudez, A.; Duato, J.; Quiles, F.J.; Sanchez, J.L.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 12 Issue: 2 , 2001
Page(s): 115 -132

[Abstract] [PDF Full-Text (324 KB)] **IEEE JRN**

7 **Overlapping decompositions and expansions of Petri nets**
Aybar, A.; Iftar, A.;
Automatic Control, IEEE Transactions on , Volume: 47 Issue: 3 , Mar 2002
Page(s): 511 -515

[Abstract] [PDF Full-Text (266 KB)] **IEEE JRN**

Copyright © 2002 IEEE — All rights reserved

Deadlock-free scheduling of flexible manufacturin systems based on heuristic search and Petri net structures

Mu Der Jeng Wan Der Chiou Yuan Lin Wen
Dept. of Electr. Eng., Nat. Taiwan Ocean Univ., Keelung;

This paper appears in: **Systems, Man, and Cybernetics, 1998. 1998 IEEE International Conference on**
10/11/1998 -10/14/1998, 11-14 Oct 1998
Location: San Diego, CA , USA
On page(s): 26-31 vol.1
11-14 Oct 1998
IEEE Catalog Number: 98CH36218
Number of Pages: 5 vol. 4945
INSPEC Accession Number: 6175793

Abstract:
Heuristic search based on Petri nets is a partial reachability graph expansion technique. The paper proposes a modified best-first algorithm and applies it t flexible manufacturing system with assembly. A heuristic function based on tl Petri net structure and dynamics is presented. It performs well especially for called generalized symmetric and asymmetric nets. The heuristic function cor of two parts. The first part estimates the total remaining operation time for a considering system dynamics. The second part approximates the maximal tot remaining operation time of each job. We begin with the first part to search t reachability tree of a timed Petri net toward an optimal or near-optimal path a depth-bound is reached. After the depth-bound, the second part is applied. also propose a one-level backtracking procedure to avoid deadlocks and a pru procedure to reduce the number of explored states. Experimental results of 1 randomly generated test cases show that this work outperforms prior work

Index Terms:
Petri nets assembling backtracking flexible manufacturing systems production contr

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A protocol for deadlock-free dynamic reconfigurat in high-speed local area networks

Casado, R. Bermudez, A. Duato, J. Quiles, F.J. Sanchez, J.L.
Dept. de Inf., Univ. de Castilla-La Mancha, Albacete;

This paper appears in: **Parallel and Distributed Systems, IEEE Transacti on**
On page(s): 115-132
Volume: 12, Feb 2001
ISSN: 1045-9219
References Cited: 23
CODEN: ITDSEO
INSPEC Accession Number: 6923065

Abstract:
High-speed local area networks (LANs) consist of a set of switches interconne by point-to-point links, and hosts linked to those switches through a network interface card. High-speed LANs may change their topology due to switches t turned on/off, hot expansion, link remapping, and component failures. In the cases, a distributed reconfiguration protocol analyzes the topology, computes new routing tables, and downloads them to the corresponding switches. Unfortunately, in most cases, user traffic is stopped during the reconfiguratio process to avoid deadlock. These strategies are called static reconfiguration techniques. Although network reconfigurations are not frequent, static reconfiguration such as this may take hundreds of milliseconds to execute, th degrading system availability significantly. Several distributed real-time applications have strict communication requirements; Distributed multimedia applications have similar, although less strict, quality of service (QoS) requirements. Both stopping packet transmission and discarding packets due the reconfiguration process prevent the system from satisfying the above requirements. Therefore, in order to support hard real-time and distributed multimedia applications over a high-speed LAN, we need to avoid stopping us traffic and discarding packets when the topology changes. In this paper, we propose a new deadlock-free distributed reconfiguration protocol that is able asynchronously update routing tables without stopping user traffic. This proto valid for any topology, including regular as well as irregular topologies. It is a valid for packet switching as well as for cut-through switching techniques and not rely on the existence of virtual channels to work. Simulation results show the behavior of our protocol is significantly better than for other protocols bas stopping user traffic

Index Terms:
local area networks packet switching protocols quality of service

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L5: Entry 1 of 11 File: USPT Jul 9, 2002

DOCUMENT-IDENTIFIER: US 6418503 B1
TITLE: Buffer re-ordering system

Abstract Text (1):
A method and implementing system is provided in which multiple nodes of a PCI bridge/router circuit are connected to corresponding plurality of PCI busses to enable an extended number of PCI adapters to be connected within a computer system. Multiple enhanced arbiters are implemented to enable non-blocking and deadlock-free operation while still complying with PCI system requirements. An exemplary PCI-to-PCI router (PPR) circuit includes the arbiters as well as PPR buffers for temporarily storing transaction-related information passing through the router circuit between adapters on the PCI busses and/or between PCI adapters and the CPUs and system memory or other system devices. A buffer re-naming methodology is implemented to eliminate internal request/completion transaction information transfers between bridge buffers thereby increasing system performance. Transaction ordering rules are also implemented along with the arbiters to enable optimal information transfer management through the buffers, and routing tables are used to enable the addressing of all of the adapters on the plurality of PCI busses, and the efficient parallel peer-to-peer and IOP transfer of information between the adapter devices and also between the system and adapter devices on the PCI busses.

Current US Cross Reference Classification (1):
710/52

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L5: Entry 1 of 11 File: USPT Jul 9, 2002

US-PAT-NO: 6418503
DOCUMENT-IDENTIFIER: US 6418503 B1

TITLE: Buffer re-ordering system

DATE-ISSUED: July 9, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Moertl; Daniel Frank	Rochester	MN		
Neal; Danny Marvin	Round Rock	TX		
Thurber; Steven Mark	Austin	TX		
Yanes; Adalberto Guillermo	Rochester	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/ 377633 [PALM]
DATE FILED: August 19, 1999

PARENT-CASE:
RELATED APPLICATIONS Subject matter disclosed and not claimed herein is disclosed and claimed in co-pending application entitled "Multiple Bus Arbiter System", Ser. No. 09/377,638, "Multi-Node PCI-to-PCI Bridge", Ser. No. 09/377,635, and "Transaction Routing System", Ser. No. 09/377,634, which are filed on even date herewith and assigned to the assignee of the present application.

INT-CL: [07] G06 F 13/10

US-CL-ISSUED: 710/310; 710/52, 710/53, 710/55, 710/57
US-CL-CURRENT: 710/310; 710/52, 710/53, 710/55, 710/57

FIELD-OF-SEARCH: 710/52, 710/53, 710/55, 710/57, 710/310

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5872941	February 1999	Goodrum et al.	370/401
☐	6219737	April 2001	Chen et al.	710/107
☐	6260095	July 2001	Goodrum	710/22

ART-UNIT: 2187

PRIMARY-EXAMINER: Nguyen; Hiep T.

ABSTRACT:

A method and implementing system is provided in which multiple nodes of a PCI bridge/router circuit are connected to corresponding plurality of PCI busses to enable an extended number of PCI adapters to be connected within a computer system. Multiple enhanced arbiters are implemented to enable non-blocking and deadlock-free operation while still complying with PCI system requirements. An exemplary PCI-to-PCI router (PPR) circuit includes the arbiters as well as PPR buffers for temporarily storing transaction-related information passing through the router circuit between adapters on the PCI busses and/or between PCI adapters and the CPUs and system memory or other system devices. A buffer re-naming methodology is implemented to eliminate internal request/completion transaction information transfers between bridge buffers thereby increasing system performance. Transaction ordering rules are also implemented along with the arbiters to enable optimal information transfer management through the buffers, and routing tables are used to enable the addressing of all of the adapters on the plurality of PCI busses, and the efficient parallel peer-to-peer and IOP transfer of information between the adapter devices and also between the system and adapter devices on the PCI busses.

26 Claims, 14 Drawing figures

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L5: Entry 2 of 11 File: USPT Sep 18, 2001

DOCUMENT-IDENTIFIER: US 6292860 B1
TITLE: Method for preventing deadlock by suspending operation of processors, bridges, and devices

Abstract Text (1):
A deadlock-avoidance system for a computer. In a multi-bus, multi-processor computer, one processor may request a lock on a bus, to execute a locked cycle, thereby blocking all other processors, and other agents, from access to the bus. In addition, a conflicting agent may, in effect, lock a resource which is needed by the processor to complete the cycle for which the lock was requested. These two locks can create a deadlock situation which stalls the computer: the processor and the conflicting agent have each locked a resource needed by the other. Under the invention, when a locked cycle is requested by a processor, all other operations are suspended in the computer. Then queues standing in memory controllers are emptied. If a process requested by an agent occupies a resource, such as a bridge, required by the requested locked cycle, that resource is freed. Then the locked cycle is executed.

Current US Cross Reference Classification (5):
711/151

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L5: Entry 2 of 11 File: USPT Sep 18, 2001

US-PAT-NO: 6292860
DOCUMENT-IDENTIFIER: US 6292860 B1

TITLE: Method for preventing deadlock by suspending operation of processors, bridges, and devices

DATE-ISSUED: September 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cochcroft, Jr.; Arthur F.	West Columbia	SC		
McDonald; Edward A.	Baton Rouge	LA		
Reams; Byron L.	Lexington	SC		
Scrivener; Harry W.	Columbia	SC		
Batchler; Bobby W.	Columbia	SC		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NCR Corporation	Dayton	OH			02

APPL-NO: 08/ 991697 [PALM]
DATE FILED: December 16, 1997

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/108; 710/101, 710/129, 710/113, 710/126, 710/200, 709/210, 711/151

US-CL-CURRENT: 710/108; 709/210, 710/113, 710/200, 710/300, 711/151

FIELD-OF-SEARCH: 710/101, 710/108, 710/200, 710/129, 710/113, 710/126, 709/210, 711/151

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4965719	October 1990	Shoens et al.	364/200
☐	4984153	January 1991	Kregness et al.	364/200
☐	5339427	August 1994	Elko et al.	395/725
☐	5408629	April 1995	Tsuchiva et al.	395/425
☐	5535365	July 1996	Barriuso et al.	395/482
☐	5625779	April 1997	Solomon et al.	710/113
☐	5717876	February 1998	Robertson	710/129
☐	5734846	March 1998	Robertson	710/113
☐	5778235	July 1998	Robertson	710/240
☐	5787486	July 1998	Chin et al.	711/163
☐	6047316	April 2000	Barton et al.	709/216

ART-UNIT: 211

PRIMARY-EXAMINER: Dharia; Rupal

ABSTRACT:

A deadlock-avoidance system for a computer. In a multi-bus, multi-processor computer, one processor may request a lock on a bus, to execute a locked cycle, thereby blocking all other processors, and other agents, from access to the bus. In addition, a conflicting agent may, in effect, lock a resource which is needed by the processor to complete the cycle for which the lock was requested. These two locks can create a deadlock situation which stalls the computer: the processor and the conflicting agent have each locked a resource needed by the other. Under the invention, when a locked cycle is requested by a processor, all other operations are suspended in the computer. Then queues standing in memory controllers are emptied. If a process requested by an agent occupies a resource, such as a bridge, required by the requested locked cycle, that resource is freed. Then the locked cycle is executed.

13 Claims, 4 Drawing figures

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L5: Entry 3 of 11 File: USPT May 1, 2001

DOCUMENT-IDENTIFIER: US 6226704 B1
TITLE: Method and apparatus for performing bus transactions orderly and concurrently in a bus bridge

Abstract Text (1):
The present invention provides a method and apparatus for performing bus transactions orderly and concurrently in a bus bridge. To meet the ordering rules, the invention adopts a HOLD/HLDA handshaking mechanism to control the flow of transactions in the bus bridge. When both HOLD and HLDA signals are asserted, the bus bridge holds the transaction processed in one direction and then the bus bridge is ready to process the transaction from another direction. That is, the bus bridge first controls the transaction flowing in one direction whenever there is request coming from another direction, wherein the HOLD signal is asserted simultaneously. Upon receipt of the HLDA signal indicating that the transaction flow has been completely held in one direction, the bus bridge allows the transaction to flow from another direction by granting the request agent bus ownership. The present invention also provides a method to avoid deadlock. The bus bridge retries transactions stalling the bus in two cases. First, the bus bridge retries non-postable transactions until the posted transactions in the posting buffers on the same side are completed at the destination. Second, the bus bridge retries postable transactions until the posting buffers on the same side have sufficient spaces to accept transactions.

Current US Cross Reference Classification (2):
709/100

Current US Cross Reference Classification (3):
710/107

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L5: Entry 3 of 11 File: USPT May 1, 2001

US-PAT-NO: 6226704
DOCUMENT-IDENTIFIER: US 6226704 B1

TITLE: Method and apparatus for performing bus transactions orderly and concurrently in a bus bridge

DATE-ISSUED: May 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wang; Wan-Kuang	Hsinchu			TW
Lin; Wen-Hsiang	Hsinchu			TW
Chen; Michael T. H.	Hsinchu			TW

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Silicon Integrated Systems Corporation	Hsinchu			TW	03

APPL-NO: 09/ 201993 [PALM]
DATE FILED: December 1, 1998

INT-CL: [07] G06 F 13/42, G06 F 13/40, G06 F 13/00

US-CL-ISSUED: 710/129; 710/128, 710/107, 709/100, 370/402
US-CL-CURRENT: 710/310; 370/402, 709/100, 710/107

FIELD-OF-SEARCH: 710/129, 710/107, 710/240, 710/2, 710/101, 710/112, 710/126, 710/128, 710/36, 710/52, 710/56.36, 710/113, 710/242, 710/105, 709/100, 711/100, 340/825.06, 370/402, 370/413, 370/462

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5761454	June 1998	Adusumilli et al.	
☐	5768547	June 1998	Ezzet	
☐	5793996	August 1998	Childers et al.	
☐	5802055	September 1998	Krien et al.	
☐	5878237	March 1999	Olarig	

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ABSTRACT:

The present invention provides a method and apparatus for performing bus transactions orderly and concurrently in a bus bridge. To meet the ordering rules, the invention adopts a HOLD/HLDA handshaking mechanism to control the flow of transactions in the bus bridge. When both HOLD and HLDA signals are asserted, the bus bridge holds the transaction processed in one direction and then the bus bridge is ready to process the transaction from another direction. That is, the bus bridge first controls the transaction flowing in one direction whenever there is request coming from another direction, wherein the HOLD signal is asserted simultaneously. Upon receipt of the HLDA signal indicating that the transaction flow has been completely held in one direction, the bus bridge allows the transaction to flow from another direction by granting the request agent bus ownership. The present invention also provides a method to avoid deadlock. The bus bridge retries transactions stalling the bus in two cases. First, the bus bridge retries non-postable transactions until the posted transactions in the posting buffers on the same side are completed at the destination. Second, the bus bridge retries postable transactions until the posting buffers on the same side have sufficient spaces to accept transactions.

29 Claims, 6 Drawing figures

WEST

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L5: Entry 4 of 11 File: USPT Sep 14, 1999

US-PAT-NO: 5951667
DOCUMENT-IDENTIFIER: US 5951667 A

TITLE: Method and apparatus for connecting expansion buses to a peripheral component interconnect bus

DATE-ISSUED: September 14, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Abramson; Darren	Folsom	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 778192 [PALM]
DATE FILED: January 2, 1997

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 710/129; 710/107
US-CL-CURRENT: 710/309; 710/107

FIELD-OF-SEARCH: 395/308, 395/309, 395/287, 395/299-305

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5555383	September 1996	Elazar et al.	395/306
☐	5675794	October 1997	Meredith	395/651
☐	5748911	May 1998	Maguire et al.	395/281

ART-UNIT: 272

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Wiley; David A.

ABSTRACT:

Modern personal computers often have several internal buses. An integrated expansion bus bridge is disclosed that couples to a fast main computer bus and couples several different expansion buses to the fast main computer bus. In one personal computer embodiment, the fast main computer bus bus is the Peripheral Component Interconnect (PCI) Bus. The expansion bus bridge obains control of the PCI bus and then arbitrates the bus control among several entities requesting access to the PCI bus. In one personal computer embodiments, the entities requesting access to the PCI bus include a Universal Serial Bus (USB) controller, an Industry Standard Architecture (ISA) bus controller, and an Integrated Drive Electronics controller. To prevent deadlock situations, the integrated expansion bus controller passively releases the PCI Bus when an ISA Direct Memory Access (DMA) operation is in progress. A passive release of the PCI bridge prevents CPU postings to or behind the expansion bus bridge from occurring. If no ISA DMA operation is in progress, then the expansion bus bridge may actively release the PCI bus.

15 Claims, 8 Drawing figures

WEST

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L5: Entry 7 of 11 File: USPT Mar 30, 1999

US-PAT-NO: 5889972
DOCUMENT-IDENTIFIER: US 5889972 A

TITLE: Bus to bus bridge deadlock prevention system

DATE-ISSUED: March 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Allingham; Donald N.	Fort Collins	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Adaptec, Inc.	Milpitas	CA			02

APPL-NO: 08/ 823958 [PALM]
DATE FILED: March 25, 1997

INT-CL: [06] G06 F 13/40, G06 F 13/14

US-CL-ISSUED: 395/308; 375/287
US-CL-CURRENT: 710/311; 710/107

FIELD-OF-SEARCH: 395/280, 395/281, 395/284, 395/287, 395/306, 395/308, 395/309, 395/310

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5542056	July 1996	Jaffa et al.	395/306
☐	5625779	April 1997	Soloman et al.	395/293
☐	5632021	May 1997	Jennings et al.	395/309

OTHER PUBLICATIONS

Digital Semiconductor 21052 PCI-to-PCI Bridge Data Sheet, Digital Equipment Corporation, pp. iii-A-2, Jan. 1996.
PCI Local Bus Specification Rev. 2.1; Jun. 1, 1995, pp. 32, 41, 43, 44, 115, and 116.

ART-UNIT: 271

PRIMARY-EXAMINER: Scheikh; Ayaz R.

ASSISTANT-EXAMINER: Pancholi; Jigar

ABSTRACT:

A bus to bus bridge deadlock prevention system detects and resolves a deadlock condition in a bus to bus bridge. In a PCI protocol application of the present invention, the system detects a retry of a request by a master device. The request is masked for a delay period before the request is allowed to attempt to pass through a PCI to PCI bridge. If the request results in a further retry, the delay period length is changed and the request is masked for the different delay period. Successive retry requests are masked for different delay periods until the deadlock condition is resolved. The system adapts to the deadlock condition by repeatedly changing the delay period until the deadlock condition is resolved and the bridged busses resume normal operation.

10 Claims, 5 Drawing figures

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L5: Entry 7 of 11 File: USPT Mar 30, 1999

US-PAT-NO: 5889972
DOCUMENT-IDENTIFIER: US 5889972 A

TITLE: Bus to bus bridge deadlock prevention system

DATE-ISSUED: March 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Allingham; Donald N.	Fort Collins	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Adaptec, Inc.	Milpitas	CA			02

APPL-NO: 08/ 823958 [PALM]
DATE FILED: March 25, 1997

INT-CL: [06] G06 F 13/40, G06 F 13/14

US-CL-ISSUED: 395/308; 375/287
US-CL-CURRENT: 710/311; 710/107

FIELD-OF-SEARCH: 395/280, 395/281, 395/284, 395/287, 395/306, 395/308, 395/309, 395/310

PRIOR-ART-DISCLOSED:

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Search Selected | Search ALL

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ART-UNIT: 271

PRIMARY-EXAMINER: Scheikh; Ayaz R.

ASSISTANT-EXAMINER: Pancholi; Jigar

ABSTRACT:

A bus to bus bridge deadlock prevention system detects and resolves a deadlock condition in a bus to bus bridge. In a PCI protocol application of the present invention, the system detects a retry of a request by a master device. The request is masked for a delay period before the request is allowed to attempt to pass through a PCI to PCI bridge. If the request results in a further retry, the delay period length is changed and the request is masked for the different delay period. Successive retry requests are masked for different delay periods until the deadlock condition is resolved. The system adapts to the deadlock condition by repeatedly changing the delay period until the deadlock condition is resolved and the bridged busses resume normal operation.

10 Claims, 5 Drawing figures

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United States Patent [19]

Kelly

[11] Patent Number: 5,996,036

[45] Date of Patent: Nov. 30, 1999

[54] **BUS TRANSACTION REORDERING IN A COMPUTER SYSTEM HAVING UNORDERED SLAVES**

[75] Inventor: **James D. Kelly**, Aptos, Calif.

[73] Assignee: **Apple Computers, Inc.**, Cupertino, Calif.

[21] Appl. No.: **08/779,632**

[22] Filed: **Jan. 7, 1997**

[51] Int. Cl.[6] G06F 9/46; G06F 13/36; G11C 7/00

[52] U.S. Cl. 710/110; 710/107; 709/208

[58] Field of Search 710/110, 107, 710/263, 41, 52; 711/151; 709/100–102, 208

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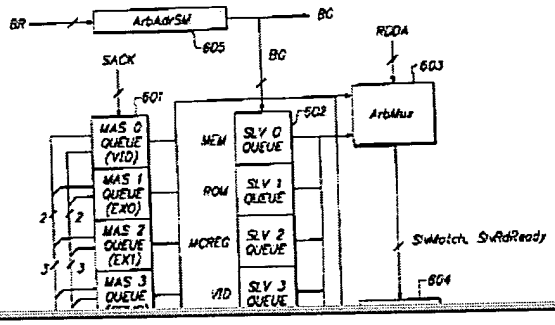
Primary Examiner—Gopal C. Ray
Attorney, Agent, or Firm—Burns, Doane, Swecker & Mathis, L.L.P.

[57] **ABSTRACT**

A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

17 Claims, 21 Drawing Sheets



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